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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,601	04/07/2004	Ping-Pang Hsieh	JCLA12197	8138

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,601	HSIEH, PING-PANG	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 9-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed 12/22/2005.

Currently, claims 9-17 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 9-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu (U. S. Patent No. 6,380,053 dated 4/30/2002) in view of Liaw (U.S. Patent No. 6,448,140 dated 9/10/2002).

Komatsu shows the structure as claimed in Figs. 3, 5A-6B, as corresponding text as: a substrate (10) (col. 12, lines 8-12); a gate structure (21) on said substrate, said gate structure including a gate dielectric layer (20) on said substrate and a gate conductive layer (21) on said gate dielectric layer (col. 12, lines 8-12); a source/drain region (23) in said substrate besides said gate structure (col. 12, lines 49-55); and an offset oxide layer (Fig. 3) on said substrate and in a portion of said source/drain region, said offset oxide layer having a bottom surface of said gate dielectric layer is apart from said gate structure and adjacent to said spacer (4nm thick silicon oxide layer) (col. 13, lines 40-58) (claim 9). Komatsu teaches that a material of said oxide spacer includes silicon oxide (col. 12, lines 13-34) (claim 10). Komatsu shows the structure as claimed in Figs. 3, 5A-6B, as corresponding text as: a gate structure (21) on said substrate (10) (col. 12, lines 8-12); a heavily doped source/drain region in a portion of the substrate exposed by the gate structure and the spacer (23) (col. 12, lines 49-55); and an offset oxide layer on the heavily doped source/drain region wherein the offset oxide layer has a bottom surface below a bottom surface of the gate dielectric layer (4nm thick silicon oxide layer) (col. 13, lines 40-58) (claim 15).

Komatsu lacks anticipation only in not explicitly teaching that: 1) an oxide spacer on a sidewall of said gate structure; a spacer on said oxide spacer; and a source/drain region in said substrate besides said gate structure and said spacer (claim 9); 2) a material said spacer includes silicon nitride (claim 11); 3) the oxide spacer has an etching selectivity relative to said spacer (claim 12); 4) a source/drain extension region formed below said oxide spacer and adjacent to said source/drain region (claim 13); 5)

a width of said oxide spacer is not larger than a width of said spacer (claim 14) 6) a spacer over the sidewall of the gate structure (claim 15); 7) an oxide layer located between the spacer and the gate structure and between the spacer and the substrate (claim 16); and 8) the offset oxide layer is an extension portion of the oxide layer and the thickness of the offset oxide layer is larger than that of the oxide layer (claim 17).

Liaw discloses a gate structure with a straight sidewall spacer. A first silicon oxide spacer (9a, 9b) is formed on both sides of a gate structure thickness 50 to 200 Angstroms and 35 to 100 Angstroms (col. 5, lines 4-28). Next a silicon nitride spacer (10) with a thickness between about 600 to 1500 Angstroms is formed on the silicon oxide spacer (col. 5, lines 29-60). The silicon nitride encapsulates the gate structure that results in smaller, higher performing MOSFET devices, with decreased source/drain to substrate capacitance (col. 1, lines 16-29).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure shown in Komatsu, an oxide spacer and of a spacer includes silicon nitride, with a selectivity relative to an oxide spacer with a with wider than the oxide spacer, as taught by Liaw, with the motivation that Liaw teaches that the gate structure that results in smaller, higher performing MOSFET devices, with decreased source/drain to substrate capacitance.

Response to Arguments

5. Applicant's arguments filed on 12/22/2005 have been fully considered but they are not persuasive. The silicon oxide of Komatsu is apart from the gate. The silicon

oxide is no longer the same material as the gate and has the offset oxide layer flowing away from the gate structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
March 1, 2006